What is claimed is:

1. A semiconductor memory device, comprising:

a plurality of normal cell blocks including a plurality of normal memory cells for storing data;

a plurality of redundancy cell blocks including a plurality of redundancy memory cells for substituting for defective normal memory cells; and

at least one ECC cell block including a plurality of ECC memory cells for substituting for the defective normal memory cells in response to a mode signal.

2. The semiconductor memory device of claim 1, wherein the plurality of ECC memory cells are used for substituting for the defective normal memory cells after each of the plurality of redundancy memory cells has been used for substituting for the defective normal memory cells.

3. The semiconductor memory device of claim 1, wherein the mode signal is generated when a bonding option occurs.

4. The semiconductor memory device of claim 1, wherein the mode signal is generated when a predetermined fuse is cut.

5. The semiconductor memory device of claim 1, further comprising:

a plurality of normal data lines for at least one of inputting and outputting the data to and from the plurality of normal memory cells;

a plurality of ECC data lines for at least one of inputting and outputting the data to and from the plurality of ECC memory cells; and

at least one repair circuit for severing a connection between at least one normal data line of the plurality of normal data lines and at least one normal cell block of the plurality of normal cell blocks in response to the mode signal, and for connecting the at least one normal data line to at least one ECC data line of the plurality of ECC data lines.

6. The semiconductor memory device of claim 5, wherein the at least one repair circuit includes:

at least one normal switching unit for controlling the connection between the at least one normal data line and the at least one normal cell block; and

at least one ECC switching unit for controlling the connection between the at least one normal data line and the at least one ECC data line.

7. The semiconductor memory device of claim 6, wherein the at least one normal switching unit and the at least one ECC switching unit are respectively turned on or off in response to control signals.

8. The semiconductor memory device of claim 7, wherein the control signals are generated when a predetermined fuse is cut or when a bonding option occurs.

9. The semiconductor memory device of claim 1, further comprising:

a plurality of normal bit lines connected to the plurality of normal memory cells;

a plurality of normal data lines for at least one of inputting and outputting the data to and from the plurality of normal memory cells;

a plurality of normal transmission gates for connecting the plurality of normal bit lines to the plurality of normal data lines in response to a first column select line signal;

a plurality of ECC bit lines connected to the plurality of ECC memory cells;

a plurality of ECC data lines for at least one of inputting and outputting the data to and from the plurality of ECC memory cells;

a plurality of ECC transmission gates for connecting the plurality of ECC bit lines to the plurality of ECC data lines in response to a second column select line signal; and

at least one repair circuit for enabling the second column select line signal in response to the mode signal.

10. The semiconductor memory device of claim 9, wherein the at least one repair circuit includes a plurality of switching units for connecting the plurality the normal data lines to the plurality of ECC data lines in response to the mode signal.

11. The semiconductor memory device of claim 10, wherein the plurality of switching units are turned on or off in response to control signals.

12. The semiconductor memory device of claim 11, wherein the control signals are generated when a predetermined fuse is cut or when a bonding option occurs.

13. The semiconductor memory device of claim 1, wherein the mode signal represents a bit configuration indicating a number of data bits one of input to and output from the semiconductor memory device.

14. A semiconductor memory device, comprising:a plurality of normal cell blocks including a plurality of normal memory cells for storing data;

at least one ECC cell block including a first plurality of ECC memory cells for storing ECC data;

at least one other ECC cell block including a second plurality of ECC memory cells, wherein the second plurality of ECC memory cells is not used for storing ECC data; and

at least one repair circuit for controlling the at least one ECC cell block and the first plurality of ECC memory cells, whereby the first plurality of ECC memory cells are used for substituting for defective normal memory cells in response to a mode signal, and are not used for storing ECC data.

15. The semiconductor memory device of claim 14, wherein the mode signal is generated in response when a bonding option occurs.

16. The semiconductor memory device of claim 14, wherein the mode signal is generated in response twhen a predetermined fuse is cut.

17. The semiconductor memory device of claim 14, further comprising:

a plurality of normal data lines for at least one of inputting and outputting the data to and from the plurality of normal memory cells; and

a plurality of ECC data lines for at least one of inputting and outputting the data to and from the first and the second plurality of ECC memory cells,

wherein the at least one repair circuit severs a connection between at least one normal data line of the plurality of normal data lines and at least one normal cell block of the plurality of normal cell blocks in response to the mode signal, and connects the at least one normal data line to at least one ECC data line of the plurality of ECC data lines.

18. The semiconductor memory device of claim 17, wherein the at least one repair circuit includes:

at least one normal switching unit for controlling a connection between the at least one normal data line and the at least one normal cell block; and

at least one ECC switching unit for controlling a connection between the at least one normal data line and the at least one ECC data line.

19. The semiconductor memory device of claim 14, further comprising:

a plurality of normal bit lines connected to the plurality of normal memory cells;

a plurality of normal data lines for at least one of inputting and outputting the data to and from the plurality of normal memory cells;

a plurality of normal gates for connecting the plurality of normal bit lines to the plurality of normal data lines in response to a first column select line signal;

a plurality of ECC bit lines connected to the first and the second plurality of ECC memory cells;

a plurality of ECC data lines for at least one inputting and outputting the data to and from the first and the second plurality of ECC memory cells; and

a plurality of ECC gates for connecting the plurality of ECC bit lines to the plurality of ECC data lines in response to a second column select line signal.

20. The semiconductor memory device of claim 19, wherein the at least one repair circuit includes at least one switching unit for connecting at least one normal data line of the plurality of normal data lines to at least one ECC data line of the plurality of ECC data lines in response to the mode signal.

21. A semiconductor memory device, comprising:

at least one first level cell block including a plurality of first level memory cells for storing data;

at least one second level cell block including a plurality of second level memory cells for substituting for defective first level memory cells; and

at least one third level cell block including a plurality of third level memory cells for substituting for the defective first level memory cells in response to a mode signal.

22. The semiconductor memory device of claim 21, wherein the plurality of third level memory cells are used for substituting for the defective first level memory cells when the plurality of second level memory cells are not available for substituting for the defective first level memory cells.

23. The semiconductor memory device of claim 21, further comprising:

at least one data line for carrying the data at least one of to and from the plurality of first level memory cells;

at least one other data line for carrying the data at least one of to and from the plurality of third level memory cells; and

at least one repair circuit for severing a connection between the at least one data line and at least one first level memory cell of the plurality of first level memory cells, and for connecting the at least one data line to the at least one other data line.

24. The semiconductor memory device of claim 21, further comprising:

at least one bit line connected to the plurality of first level memory cells;

at least one data line for carrying the data at least one of to and from the plurality of first level memory cells;

at least one transmission gate for connecting the at least one bit line to the at least one data line in response to a first column select line signal;

at least one other bit line connected to the plurality of third level memory cells;

at least one other data line for carrying the data at least one of to and from the plurality of third level memory cells;

at least one other transmission gate for connecting the at least one other bit line to the at least one other data line in response to a second column select line signal; and

at least one repair circuit for enabling the second column select line signal in response to the mode signal.